

Appl. No. 10/697,131

REPLY UNDER 37 C.F.R. 1.116
Expedited Procedure
Technology Center - 2816**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of distributing a clock signal over a transmission line, the method comprising:

- providing a return line geometrically matched to the transmission line;
- generating an output clock signal onto a transmission line;
- detecting a returned clock signal on the return line;
- detecting a first phase difference between a reference clock signal and the output clock signal;
- detecting a second phase difference between the reference clock signal and the returned clock signal;
- controlling the phase of the output clock signal based on an average of the first and second phase differences.

2. (currently amended) ~~A method, as set forth in claim 1, further comprising A~~
method of distributing a clock signal, the method comprising:

- generating an output clock signal onto a transmission line;
- ~~detecting a returned clock signal by sensing a reflection of the~~
output clock signal on the transmission line;
- detecting a first phase difference between a reference clock signal and the output clock signal;
- detecting a second phase difference between the reference clock signal and the returned clock signal;
- controlling the phase of the output clock signal based on an average of the first and second phase differences.

3. (canceled)

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4. (previously presented) A method, as set forth in claim 2, wherein the reflected signal is sensed by comparing the output clock signal with a composite signal from the transmission line, the composite signal including the output clock signal and a reflection of the output clock signal from the destination.
5. (previously presented) A method, as set forth in claim 1, wherein the step of controlling the phase of the output clock signal comprises driving a voltage controlled oscillator using the average of the first and second phase differences.
6. (previously presented) A method, as set forth in claim 5, further comprising buffering the output of the voltage controlled oscillator.
7. (currently amended) ~~A method, as set forth in claim 5, further comprising A~~
method of distributing a clock signal, the method comprising:
_____ generating an output clock signal onto a transmission line;
_____ detecting a returned clock signal;
_____ detecting a first phase difference between a reference clock signal and the
output clock signal;
_____ detecting a second phase difference between the reference clock signal and
the returned clock signal;
_____ controlling the phase of the output clock signal based on an average of the
first and second phase differences by driving a voltage controlled oscillator using the
average of the first and second phase differences; and
_____ buffering the output of the voltage controlled oscillator and providing a build
out impedance to match the transmission line impedance.
8. (canceled)

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9. (currently amended) ~~The A~~ clock distribution circuit, ~~as set forth in claim 8~~, further comprising:

a first phase detector that outputs a phase lead of an output clock signal;
a second phase detector that outputs a phase lag of a returned clock signal;
circuitry that propagates the output clock signal onto a transmission line
based on the average the output of the first phase detector and the second phase
detector; and
circuitry to ~~detect~~ detect the returned clock signal as a reflected clock signal on the transmission line.

10. (currently amended) ~~The A~~ clock distribution circuit, ~~as set forth in claim 8~~, further comprising:

a first phase detector that outputs a phase lead of an output clock signal;
a second phase detector that outputs a phase lag of a returned clock signal;
circuitry that propagates the output clock signal onto a transmission line
based on the average the output of the first phase detector and the second phase
detector; and
a signal return line separate from the transmission line, wherein the returned clock signal is sensed from the signal return line.

11. (previously presented) The clock distribution circuit, as set forth in claim 10, wherein the signal return line is matched to the transmission line.

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12. (previously presented) A clock distribution system comprising:

a reference clock that output a clock signal;

a first clock distribution circuit comprising:

a first phase detector that outputs a phase lead of a first output clock signal;

a second phase detector that outputs a phase lag of a first returned clock

signal; and

first circuitry that propagates the first output clock signal onto a first transmission line based on the average the output of the first phase detector and the second phase detector;

a second clock distribution circuit comprising:

a third phase detector that outputs a phase lead of a second output clock

signal;

a fourth phase detector that outputs a phase lag of a second returned clock signal; and

second circuitry that propagates the first output clock signal onto a second transmission line based on the average the output of the third phase detector and the fourth phase detector; and

wherein the first transmission line is a different length than the second transmission line and the first and second output clock signals coincide at the end of the first and second transmission line.

13. (previously presented) A method of distributing a reference clock signal, the method comprising:

sensing an output clock signal to be sent over a transmission line;

sensing a reflected clock signal at the beginning of the transmission line; and

adjusting the output clock signal based on an average of a first phase difference between the output clock signal and the reference clock signal and a second phase difference between the reflected clock signal and the reference clock signal.

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14. (previously presented) A method of distributing a reference clock signal, the method comprising:

sensing an output clock signal to be sent over a transmission line;

sensing a returned clock signal at the end of a signal return line matched to the transmission line; and

adjusting the output clock signal based on an average of a first phase difference between the output clock signal and the reference clock signal and a second phase difference between the returned clock signal and the reference clock signal.